TITLE

Please amend the title as follows:

PROCESSOR AND METHOD OF EXECUTING A LOAD INSTRUCTION THAT BIFURCATE LOAD EXECUTION INTO ~~TWO~~ PREFETCH AND REGISTER OPERATIONS

SPECIFICATION

Please amend Table I at page 11 as follows:

A1

TABLE I

	Cycle 1	Cycle 2	~~Cycl e~~ Cycle 3	Cycle 4	~~Cycl e~~ Cycle 5	Cycle 6	Cycle7
ADD1	D	X	C				
PRE	D	X		pre-fetch data to L1 data cache			
SUB1		D	X	C			
MUL1		D	X	C			
MUL2			D	X	C		
ST			D	X	C		
SUB2				D	X	C	
REG				D	X	C	
ADD2					D	X	C